Claims

We Claim:

1. A lateral FET structure comprising:

a body of semiconductor material having a first conductivity type;

a first well region of a second conductivity type formed in the body of semiconductor material;

a second well region of the second conductivity type formed the body of semiconductor material;

a first drain contact region of the second conductivity type formed in a portion of the first well region;

a second drain contact region of the second conductivity type formed in a portion of the second well region;

a first doped region of the first conductivity type formed in another portion of the body of semiconductor material adjacent to the first well region;

a first source region of the second conductivity type formed in the first doped region;

a gate structure formed over the first major surface;

a first conductive layer coupled to the first source region to form a source contact;

a second conductive layer formed over the body of semiconductor material and coupled to the first and second drain contact regions; and

an interlayer dielectric layer separating at least a portion the first and second conductive layers.

2. The structure of claim 1 wherein the first doped region surrounds the first well region.

3. The structure of claim 1 further comprising a second source region formed in the doped region, and wherein the first conductive layer is coupled to the second source region.

4. The structure of claim 1 further comprising a second doped region of the first conductivity type surrounding the second well region, and wherein the first and second doped regions are absent a fingertip region.

5. The structure of claim 1 wherein the first drain region comprises an elongated stripe shape.

6. The structure of claim 5 wherein the first source region comprises an elongated stripe shape substantially parallel to the first drain region.

7. The structure of claim 1 wherein the first and second well regions are spaced apart.

8. The structure of claim 1 wherein the first well region includes a pair of opposing rounded tips.

9. The structure of claim 1 further comprising a second doped region of the first conductivity type formed in a portion of the first well region adjacent to the first drain region.

10. The structure of claim 1 wherein the first conductive layer and second conductive layer do not overlap.

11. The structure of claim 1 wherein a portion of the second conductive layer is over a portion of the first well region and separated from the first well region by a dielectric layer.

12. A lateral FET device comprising:

a body of semiconductor material having a first conductivity type;

a plurality of drain regions of a second conductivity type, formed in the body of semiconductor material;

a plurality of source regions of the second conductivity type formed in the body of semiconductor material;

a first conductive layer formed over the body of semiconductor material and coupled to the plurality of drain regions;

a second conductive layer formed over the body of semiconductor material and coupled to the plurality of source regions; and

a dielectric layer formed over the body of semiconductor material, wherein one of the first and second conductive layers is formed over the dielectric layer.

13. The device of claim 12 wherein the plurality of drain regions comprises a plurality of well regions and a plurality of drain contact regions, and wherein at least one drain contact region is formed within one well region.

14. The device of claim 12 wherein the first and second conductive layers do not overlap.

15. The device of claim 12 further comprising a plurality of doped regions of the first conductivity type, wherein one of the plurality of source regions is within one of the plurality of doped regions, and wherein one of the plurality of doped regions surrounds one of the plurality of well regions.

16. The device of claim 12 wherein portions of the second conductive layer terminate in proximity to the first conductive layer.

17. A method for forming a lateral FET device comprising the steps of:

providing a body of semiconductor material having a first conductivity type;

forming a plurality of drain regions in the body of semiconductor material;

forming a plurality of source regions in the body of semiconductor material;

forming a first conductive layer on the body of semiconductor material and coupled to the plurality of drain regions; and

forming a second conductive layer on the body of semiconductor material and coupled to the plurality of source regions, wherein at least a portion of the second conductive layer is separated from a portion of the first conductive layer by a dielectric layer.

18. The method of claim 17 wherein the step of forming the plurality of drain regions comprises the steps of:

forming a plurality of well regions in the body of semiconductor material, and

forming a drain contact region in at least one of the plurality of well regions.

19. The method of claim 18 further comprising a step of forming a first conductivity type doped region in at least one of the plurality of well regions.

20. The method of claim 17 wherein the step of forming the second conductive layer includes forming a second conductive layer wherein portions of the second conductive layer terminate in proximity to the first conductive layer.